WEST Search History

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☐	L1	(without near3 (outside or external$4) near3 (storage or memory))	1663

END OF SEARCH HISTORY

L2: Entry 3 of 6 File: USPT Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5802550 A
TITLE: Processor having an adaptable mode of interfacing with a peripheral storage device

Brief Summary Text (9):
Because each new type of memory device employs device-specific data formatting and control timing, system designers usually design a processor system with a particular memory device and clock speed in mind. As a result, hardware and software control of external memory devices is typically fixed within a given processor system. This can lead to difficulty should a designer wish to change memory parts or processor speed at a late stage in the design process. A designer might wish to change memory parts when a certain part ceases to be available, when a faster part suddenly becomes available, or when a faster CPU is desired in the system. If a processor system is configured to work only with a certain type of memory part and clock speed, then switching to a new part or changing the clock speed requires a time-consuming and expensive re-design effort. However, if the processor system could be configured to include adjustable memory timing control, then switching to a new memory part or clock speed would require only that the processor be re-adjusted or re-programmed. In the past, processors have been designed to provide user-programmable control of a memory device. For example, U.S. Pat. No. 5,386,385 discloses a processor comprising a mode register storing data relating to certain operations of a synchronous dynamic RAM (SDRAM). Specifically, the user can designate the length of a data burst, and whether the SDRAM is to operate in a serial or interleaved mode. Once the SDRAM is so programmed, it operates in that manner each subsequent time the processor boots up. This approach is designed to work with the specific SDRAM connected to the processor, and is not intended to accommodate different types of memory devices. Thus, there is a need for a method and an apparatus by which a digital processor can automatically adapt to correctly interface with a variety of external memory devices, without requiring user input or system redesign.